REMARKS

This Amendment seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed. Claims 151-201 are pending. Several of the pending claims have been amended. No new matter has been added.

It should be mentioned that the amendments made to claim 173 in the Amendment dated December 17, 2002 were not properly reflected in the subsequent Amendment dated April 3, 2002, which inadvertently presented claim 173 as it appeared prior to the Dec. 17 Amendment. The set of claims presented herein in clean form include claim 173 as amended in the Dec. 17 Amendment.

OFFICE ACTION

In the Office Action mailed July 31, 2002 (hereinafter, "the OFFICE ACTION"), claim 151-201 were rejected[1] under 35 U.S.C. §112, first paragraph. In this regard, the Examiner stated:

> Applicant failed to provide an adequate written description to how the first operation code is sampled as claimed in claims 151-163, 173-192 and 197-201. It appears that only the clock signal and the input data are sampled.
>
> It is not clear how the first operation code initiates an access of the programmable register as claimed in claims 164-172 and 193-196. It appears that the first operation code initiates the read operation.

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1 Previously, in the office action dated March 13, 2002, claims 151-163 were indicated as allowed.

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Applicants submit that the specification, as filed, fully supports "how the first operation code is sampled as claimed in claims 151-163, 173-192 and 197-201".

In several embodiments described in the specification as filed, input receivers within the memory device sample the operation code. In one embodiment, the operation code is sampled synchronously with respect to an external clock signal (see, "AccessType[0:3]", which is sampled at "CYCLE 0" in Figure 4 and page 22, lines 11-13, page 54, lines 3-8). In another embodiment, the operation code is sampled upon a transition of an internal device clock. (e.g., one of internal device clocks 73 and 74 in Figures 10 and 13; and page 58 lines 18-21). The internal device clocks are generated within the memory device using an external clock signal. (see, page 57, lines 3-25, page 58, lines 16-21 and Figure 13.) Here, the internal device clocks are synchronized with edge transitions of the external clock signal (see, page 58, lines 1-18 and Figure 13).

Applicants submit that the specification, as filed, fully supports how the "first operation code initiates an access of the programmable register as claimed in claims 164-172 and 193-196."

The specification describes several embodiments in which semiconductor device(s) (e.g., semiconductor memory devices) include "a set of internal registers, preferably including a device identification (device ID) register, a device-type descriptor register, control registers and other registers containing other information relevant to that type of device." (see page 14, lines

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3-7). In an embodiment, several of these registers are programmed in response to an operation code. (see page 23, lines 12-21; see also, page 14, lines 13-21; and page 35, line 23 to page 36, line 1).

In one embodiment, the operation code is "AccessType[0:3]" (see page 22, lines 12-13). "The AccessType field specifies ... the type of access, for example, whether it is to control registers ...." (see page 22, lines 19-21)).

When the operation code initiates an access to the register in order to store data in the register, the memory device responds by storing the data (i.e., the value) in the register. In this regard, the specification states:

> One special type of access is control register access, which involves addressing a selected register in a selected slave. In the preferred implementation of this invention, AccessType [1:3] equal to zero indicates a control register request and the address field of the packet indicates the desired control register. For example... the least significant three bytes can specify a register address and may also represent or include data to be loaded into that control register. (page 23, lines 12-21)

Applicants submit that every feature of pending claims 151-201 is fully supported by the application as filed.

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Information Disclosure Statement

Applicants draw the Examiners attention to an Information Disclosure Statement (submitted under 37 CFR 1.97(c)), citation form PTO-1449 and a copy of each document cited therein, which was mailed on Nov. 14, 2002. As a courtesy, a copy of this Information Disclosure Statement and citation form PTO-1449 is attached hereto.

It is respectfully requested that the Examiner make his consideration of these submissions formally of record with the next Action.

Conclusion

Applicants request reconsideration of the instant application in view of the foregoing remarks and amendments. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

Respectfully submitted,

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Exhibit A -- Version with Markings to Show Changes Made

151. (Amended) A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells and a programmable register, the method of operation of the memory device comprises:

sampling a first operation code synchronously with respect to a transition of an external clock signal;

receiving a binary value synchronously with respect to the external clock signal, wherein the binary value is representative of a delay time to transpire before the memory device is to output data in response to a second operation code, wherein the second operation code [initiates] specifies a read operation [in] to the memory device; and

storing the binary value in the programmable register in response to the first operation code.

158. (Twice Amended) The method of claim 151 further including:

receiving block size information, wherein the block size information is representative of an amount of data to be output;

receiving the second operation code; and

outputting the amount of data, in response to the second operation code, after the delay time transpires.

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159. (Amended) The method of claim 158 wherein the block size information further defines an amount of data to be input in response to a third operation code, wherein the third operation code [initiates] specifies a write operation [in] to the memory device, the method further including:

receiving the third operation code; and

inputting the amount of data in response to the third operation code.

162. (Amended) The method of claim [155] 151 further including:

receiving the second operation code; and

outputting data in response to the second operation code, wherein the data is output synchronously with respect to consecutive rising and falling edge transitions of the external clock signal.

163. (Amended) The method of claim 151 wherein the first operation code is received [in] during an initialization sequence after power is applied to the memory device.

164. (Twice Amended) A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells and a programmable register, the method of controlling the memory device comprises:

issuing a first operation code to the memory device, wherein the first operation code [initiates] specifies an access of the programmable register in the memory device in order to store a binary value, wherein the binary value is representative of control information; and

providing the binary value to the memory device, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

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172. (Amended) The method of claim [164]171 wherein the first operation code and the binary value are included in the same request packet.

174. (Twice Amended) The memory device of claim 173 wherein the control information is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs data, and wherein the memory device outputs the data in response to a second operation code.

176. (Thrice Amended) The memory device of claim 173 further including a plurality of output drivers to output data[, wherein the data is output] in response to a second operation code, wherein the second operation code specifies [that initiates] a read operation, and wherein the plurality of output drivers output a first portion of the data synchronously with respect to a rising edge transition of the external clock signal and output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

178. (Amended) The memory device of claim 173 wherein the first operation code and the binary value are each included in a request packet.

180. (Twice Amended) The memory device of claim 173 wherein the plurality of input receivers are operative to receive a second operation code, wherein the second operation code [initiates] specifies a write operation to [in] the memory device, and wherein the memory device further includes[:]additional input receivers to input data in response to the second operation code.

192. (Amended) The memory device of claim 191 wherein the [memory device includes] programmable register is included in a

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plurality of programmable registers of the memory device, each register of the plurality of registers to store a corresponding binary value.

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